# Embedded Dynamic Clamp Requirements

The dynamic clamp (DC) is a real time, closed loop device to couple voltage gated conductances in a cell with simulated conductances to create a hybrid cell. We require

1. A device that is fast enough to interact with sodium channels
2. Can be incorporated into a high throughput automated electrophysiology platform
3. Present the simplest possible interface to the user

## Basic configuration

Our assumption is that the best way to achieve this is by having the DC in a separate device. Two example configurations are shown in Fig 1. In the first configuration (Fig 1A), the experimental workstation interacts with the patch clamp amplifier as it would for standard voltage clamp experiments. In the second configuration, the host interacts directly with the DC.

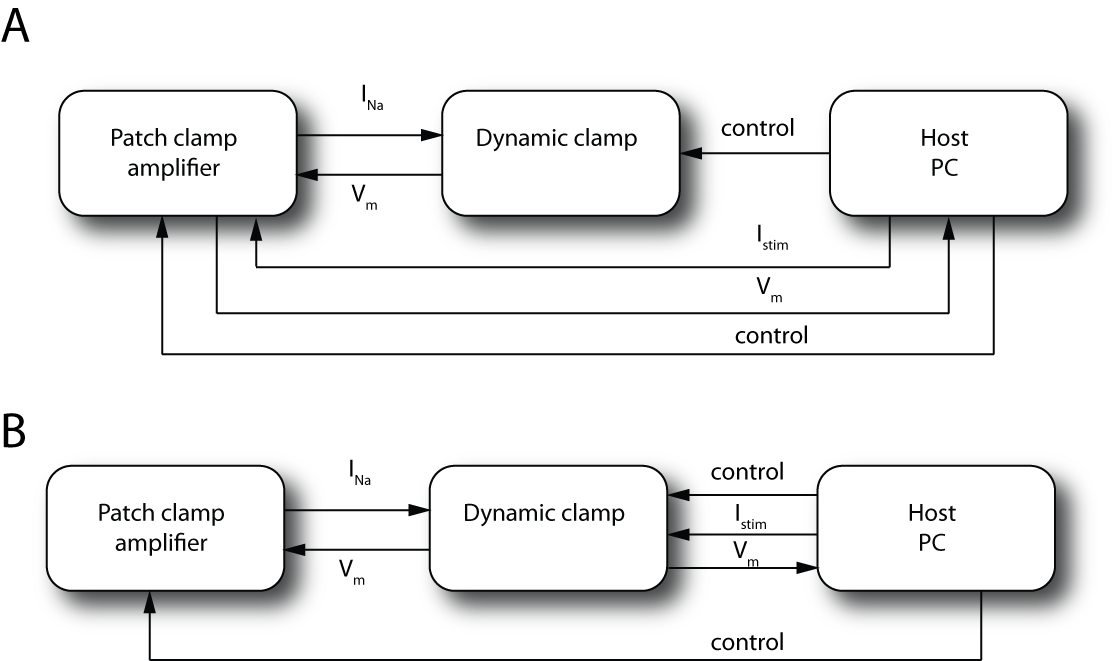


Figure . An example DC configurations, running in voltage clamp mode, to interact with a cell expressing sodium channels. *Vm* is the membrane potential, *INa* is sodium current measured from the real cell. *Istim* is a stimulus, for example a current step. Control signals set device configuration, download parameters and provide triggering. *A)* Standard software on the host interacts directly with the amplifier to stimulate the cell and capture output. *B)* The host interacts directly with the DC to provide stimuli and read output.

Experimental workflow consists of three phases: amplifier configuration; cell characterisation and DC configuration; experiment. In the first phase cell access resistance, cell leak conductance, cell capacitance, pipette capacitance and any offsets are determined and the amplifier is configured to compensate for access resistance and subtract capacitive currents and leak. This occurs when the cell is first patched and needs to be performed periodically as the parameters drift over time. The DC is very sensitive to inadequate compensation and quality of current automatic compensation in, for example HEKA amplifier, is not adequate. In the second phase standard voltage clamp protocols are applied to the cell to characterise the expressed current. This determines basic viability of the cell and provides parameters such as maximum current that are required by the DC. It also provides “standard” data that can be compared against DC output. The DC needs to be aware of other conditions such as cell holding potential so that the cell is not subject to large voltage jumps when the apparatus switches between modes. In the third phase, the DC is configured to run with the currently patched cell and current stimuli are applied to the hybrid cell.

## Main signal flow

Fig 2 indicates the signal flow. In standard voltage clamp experiments low pass filtering is performed by low order analogue filters in the amplifier however there will considerable benefit to performing this filtering in the DC. The anticipated sample time of the DC is anticipated to be high compared to the sample time required for analysis and display. There may also be a bandwidth limitation transferring say 8 channels of DC data over a USB port. Therefore the DC will need to down sample data prior to transfer to the host.

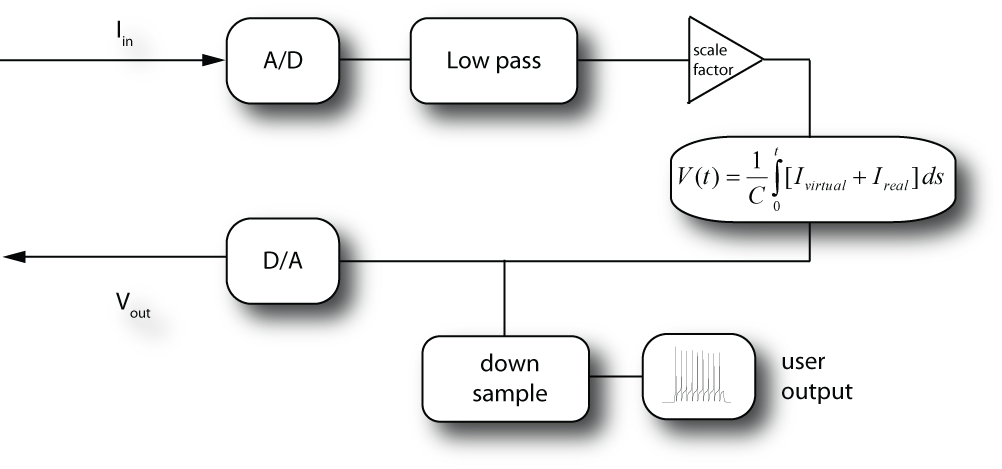


Figure . Signal flow during real time interaction between the DC and cell.

## Mathematical models

The models that we solved on the DC are subclass of membrane model known as Hodgkin-Huxley (HH) models. These look like

 (1)

where *Cm* is the membrane capacitance, *V* is the membrane potential. There are several ionic currents and in HH models these take the form

 (2)

*VR*is the reversal potential, *g* is the maximum conductance and *ek* are integer exponents. These are model parameters provided by the experimenter. *nk* are the *gating* variables and described by an equation of the form

 (3)

where *n∞* and *τn* are functions of voltage and are also provided by the experimenter. *Istim(t)* is a stimulus provided by the experimenter, for example a step function.

In a hybrid cell, some currents are provided by a real biological cell and some currents are simulated in the DC. In *voltage clamp* mode, the cell membrane voltage is calculated in the DC, used to the command the cell membrane the corresponding current is feed back into the model.

 (4)

where *fscale* scales the cell current to match the conductance required for the hybrid cell. The stimulus might generated in the DC or applied externally or be a combination of both.

In *current clamp* mode the membrane potential is read from the real cell, fed into the model, ionic currents are calculated passed across the cell membrane.

 (5)

Six currents should be adequate, there are never more than 3 gates per current and the gate exponent will always be 4 or less. In HH models, the gates and currents are independent and can be solved in parallel.

In later versions of the DC, there will be coupling between currents by intracellular calcium and other signally mechanisms. We will also need to use Markov models to describe channel gating.

During testing, debugging and for some research projects it will be necessary to upload gating variables and currents as a function of time.

## Host software

Host software is required for the following functions.

A tool is needed for model definition. The tool should enable and encourage a workflow whereby models are tested for correctness as they are converted from the primary source (e.g. Matlab, Simulink or NEURON) into the format required by the tool and then compared to model execution on the DC.

Once models are built and tested they can be stored on disk and downloaded to the DC as required. Initially a single model will be downloaded to the DC prior to a series of runs, however in later versions it may be advantageous to test individual cells in several models.

As mentioned, current amplifier automatic configuration for isolating the relevant current is either not adequate for DC experiments or in the case of the Alembic amplifier does not exist. For ease of development we propose initially determining and applying amplifier configuration on the host.

Host software requires access the output of voltage clamp protocols to determine characteristics of the currently patched cell such as maximum current. The host software can then set parameters in the DC.

The host software needs to be integrated into the automation software so that amplifier configuration, DC configuration and switching DC modes can be performed at the appropriate times during the experimental runs.